

ABSTRACT OF THE DISCLOSURE

An interrupt signal processing apparatus, when receiving an interrupt
5 requesting signal from one device, writes a pulse signal generated by an
interrupt setting pulse generating section to a register. The interrupt signal
processing apparatus, when receiving an interrupt clearing request signal
from the other device, clears the register by using a pulse signal fed from the
interrupt clearing pulse generating section and outputs the interrupt
10 permission signal to the one device. When a clock speed of the other device is
lower than that of the one device and when pulse generation is controlled by
a control signal fed from the clearing pulse generating section of the other
device, while the pulse signal fed from the other device is input to the delay
circuit, a time delay is provided to operations of the second synchronization
15 section. Thus, smooth interruption can be implemented regardless of the
clock speed.